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Design of Multiplier less circuit for image compression using DCT

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ABSTRACT

In this paper, a different hardware implementation for image compression using DCT algorithm is analyzed, like, multiplier-less circuit designs and performance characteristics. Implementation techniques reviewed include designs based on device utilization, computational complexity, power consumption and delay. It was noted from the survey that multiplier less circuit employing 14 adder circuits is efficient than the other designs in terms of retaining their image quality. Also, the proposed system is found to have better performance characteristics proving to be more reliable and efficient in image processing applications.

KEY WORDS: DCT algorithm, device utilization, performance characteristics, image processing.

1. INTRODUCTION

One of the many techniques under image processing is image compression. Recent years have experienced a significant demand for high dynamic range systems that operate at high resolution. There are many compression standards among which the Discrete Cosine Transform (DCT) is an essential mathematical tool in both image and video coding. DCT was demonstrated to provide good energy compaction properties. In order to replace the poor image quality reconstruction of the image in DCT, multiplier-free approximate transforms have been proposed that offer superior compression performance at very low circuit complexity, leading to reduce the chip area and power consumption compared to conventional DCTs and integer transforms. The Comparison is done in terms of both algorithm complexity and performance characteristics. This paper proposes to review some such papers that are based on various algorithms involved.

Related Works: The format in which the transformation matrix is formed can be put as [Diagonal matrix] x[low complexity matrix] Here the diagonal matrix consists of irrational numbers $1/\sqrt{m}$ where m is a positive integer. These irrational numbers require an increased computational complexity. During image compression, this diagonal matrix is absorbed into the quantization step thus limiting its complexity. The complexity of the approximation is bounded by the complexity of the low complexity matrix. Null multiplicative complexity is achieved since the entries of the low complexity matrix comprise only powers of two.

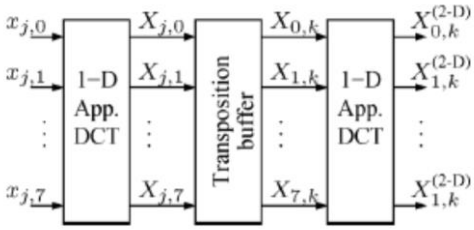

Figure.1. Two-dimensional block transform for 8 x 8 matrix compression

The general DCT algorithm is performed as described below in the figure.

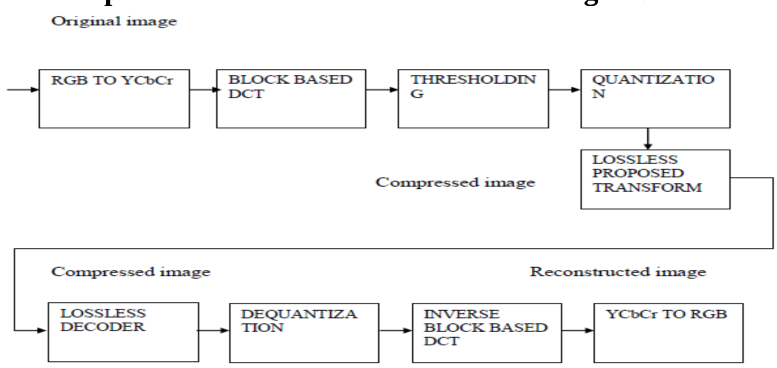

Figure.2. DCT algorithm description

Bouguezel-Ahmad-Swamy Approximate DCT: An efficient 8 X 8 sparse orthogonal transform matrix was proposed for image compression by appropriately introducing some zeros in the 8 X 8 signed discrete cosine transform (SDCT) matrix. The existing system (Bouguezel, 2008) consists of approximating the DCT by applying a signum function operator to the forward DCT matrix in order to obtain a matrix the entries of which are only 1, 0 or

21; the resulting SDCT still has good de-correlation and power compaction properties. The proposed 8 X 8 transform matrix is obtained by appropriately introducing some 0s and 1/2 s in the 8 X 8 SDCT matrixes.

$$\mathbf{C_1} = \mathbf{D_1} \cdot \mathbf{T_1}$$

$$= \mathbf{D_1} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & -1 & -1 \\ 1 & \frac{1}{2} & -\frac{1}{2} & -1 & -1 & -\frac{1}{2} & \frac{1}{2} & 1 \\ 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 1 & -1 \\ \frac{1}{2} & -1 & 1 & -\frac{1}{2} & -\frac{1}{2} & 1 & -1 & \frac{1}{2} \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

$$D = \mathrm{diag}\left(\frac{1}{2\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{5}}, \frac{1}{\sqrt{2}}, \frac{1}{2\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{5}}, \frac{1}{\sqrt{2}}\right)$$

The forward and inverse transformation operations can be performed using the proposed transform as

$F = CXC^t = D\,(TXT^t)\,D$, $X = C^tFC = T^t\,(DFD)\,T$, respectively.

The matrix can be decomposed as$T = T3 \times T2 \times T1$

Parametric Transform: A one-parameter eight-point transform (Bouguezel, 2011) was proposed by introducing an arbitrary parameter in the transform matrix and performing some row permutations. The elements of the transform matrix that are replaced by the parameter are appropriately selected to ensure the orthogonality property of the resulting parametric transform. The purpose of the row permutations is to enhance the energy compaction capability of the transform. This process leads to a new transform matrix given by

$$\mathbf{C^{(a)} = D^{(a)} \,.\, T^{(a)}}$$

$$= \mathbf{D}^{(a)} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 & -1 & -1 \\ 1 & a & -a & -1 & -1 & -a & a & 1 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 1 & -1 \\ a & -1 & 1 & -a & -a & 1 & -1 & a \end{bmatrix}$$

Where *a* is an arbitrary scalar, $D_a$is a diagonal matrix given by

$$D_a = \mathrm{diag}\left(\frac{1}{\sqrt{8}}, \frac{1}{\sqrt{4}}, \frac{1}{\sqrt{4+4a2}}, \frac{1}{\sqrt{2}}, \frac{1}{\sqrt{8}}, \frac{1}{\sqrt{2}}, \frac{1}{\sqrt{4}}, \frac{1}{\sqrt{4+4a2}}\right)$$

Ca is orthogonal for all possible values of a i.e. $C_a^{-1} = C_a^t = T_a^t D_a$

Where t denotes the transpose operation. The matrix T_a is the only source of arithmetic operations in the transformation step of an image compression procedure. The direct transformation of an eight-element row or column vector using T_a requires 36 additions and 8 multiplications. In order to reduce this computational complexity, a fast algorithm was developed valid for any value of the parameter *a* by decomposing T_a into a product of sparse matrices in the form$T_a = P \times Q_a \times R \times S$

CB-2011 Approximation: The CB-2011 method (Cintra, 2011) modifies the standard DCT matrix C by means of the rounding-off operation. Initially, matrix C is scaled by two and then submitted to an element-wise round-off operation. Let [.] denote the round-off operation as implemented in Mat lab programming environment. Thus, the resulting matrix,

$C_0 = [2.C]$

$$\mathbf{C_2} = \mathbf{D_2} \cdot \mathbf{T_2}$$

$$= \mathbf{D_2} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & -1 & -1 & -1 \\ 1 & 0 & 0 & -1 & -1 & 0 & 0 & 1 \\ 1 & 0 & -1 & -1 & 1 & 1 & 0 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & 0 & 1 & -1 & 0 & 1 & -1 \\ 0 & -1 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & -1 & 1 & -1 & 1 & -1 & 1 & 0 \end{bmatrix}$$

However, the suggested approximation has some drawbacks: i) it lacks orthogonality, since$C_0^{-1} \neq C_0^T$ where superscript denotes matrix transposition ii) its resulting approximation is poor when compared with some existing methods. Considering matrix polar decomposition, an adjustment matrix S that orthogonalizes C0 is sought. The referred orthogonalization matrix is given by

$$S = \sqrt{(C_0 . C_0^T)}^{-1}$$

$$S = \mathrm{diag}\left(\frac{1}{2\sqrt{2}}, \frac{1}{\sqrt{6}}, \frac{1}{2}, \frac{1}{\sqrt{6}}, \frac{1}{2\sqrt{2}}, \frac{1}{\sqrt{6}}, \frac{1}{2}, \frac{1}{\sqrt{6}}\right)$$

The DCT matrix can be more adequately approximated by the following proposed matrix $C_{ORTH} = S.C_0$. The transfer function related to each row of a given transformation matrix T could be calculated according to$H_m(w; T) = \sum_{n=0}^{7} t_{m,n} \exp(-jnw)$, where m=0 to 7, $j = \sqrt{-1}$, $w \in [0, \pi]$

Modified CB-2011 Approximation: The modified CB-2011 approximation is obtained by judiciously replacing elements of the CB-2011 matrix with zeros, we obtained T (Bayer, 2012). The approximation is expressed by

$C = D.T$

$$\mathbf{C_3} = \mathbf{D_3} \cdot \mathbf{T_3}$$
$$= \mathbf{D_3} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & -1 & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 0 & -1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & -1 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

$$D = \mathrm{diag}\left(\frac{1}{\sqrt{8}}, \frac{1}{\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{2}}, \frac{1}{\sqrt{8}}, \frac{1}{\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{2}}\right)$$

The entries of T are {0, +1}. This is an attestation of its null multiplicative complexity. Moreover, bit-shift operations are fully absent. Not only does C inherit the low computational complexity of T, but it is also orthogonal. In terms of complexity assessment, matrix D may not introduce any computational overhead. Matrix D, in the form of D2, can be merged into the quantization matrix. Moreover, all elements of D2 are negative powers of two {1/2, 1/4, 1/8}. Therefore, any implementation of the quantization step for the exact DCT can be easily adapted to the proposed method by adequately bit-shifting the elements of the quantization matrix. A fast algorithm based on sparse matrix factorization leads to T = P. A3. A2. A1

Approximate DCT: A DCT approximation (Potluri, 2012) tailored for a particular radio frequency (RF) application was obtained in accordance with an exhaustive computational search. This transformation is given by

$$\mathbf{C_4} = \mathbf{D_4} \cdot \mathbf{T_4}$$
$$= \mathbf{D_4} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 2 & 1 & 1 & 0 & 0 & -1 & -1 & -2 \\ 2 & 1 & -1 & -2 & -2 & -1 & 1 & 2 \\ 1 & 0 & -2 & -1 & 1 & 2 & 0 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -2 & 0 & 1 & -1 & 0 & 2 & -1 \\ 1 & -2 & 2 & -1 & -1 & 2 & -2 & 1 \\ 0 & -1 & 1 & -2 & 2 & -1 & 1 & 0 \end{bmatrix}$$

$$D_4 = ½.\ \mathrm{diag}\left(\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{3}}, \frac{1}{\sqrt{5}}, \frac{1}{\sqrt{3}}, \frac{1}{\sqrt{2}}, \frac{1}{\sqrt{3}}, \frac{1}{\sqrt{5}}, \frac{1}{\sqrt{3}}\right)$$

The fast algorithm for its computation consists of the following matrix factorization$T_4 = P_3 .A_9 .A_8 .A_1$.
This method employs 26 addition operations with 6 shift operation to perform image compression.

2. METHODS AND MATERIALS USED IN MULTIPLIER CIRCUIT

Multiplierless Circuit Employing 14 Additions: A novel based low complexity DCT is proposed with an 8 x 8 matrix. In order to have low computational cost, the number of arithmetic operations required for its computation is reduced.

$$\mathbf{T}^* = \underset{\mathbf{T}}{\mathbf{arg\ min\ cost}}\ (\mathbf{T})$$

Where T* is the sought matrix, cost (T) returns the arithmetic computation cost. The elements of matrix T consists of {0,±1,±2}, thus ensuring null multiplicative complexity. An important parameter considered is the number of retained coefficients in the transform domain. Generally, the number of retained coefficients is low. As suggested in [1] the number of coefficients considered is equal to 10.

$$\mathbf{C}^* = \mathbf{D}^* \cdot \mathbf{T}^*$$
$$= \mathbf{D}^* \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \end{bmatrix}$$

Where $D^* = \mathrm{diag}\left(\frac{1}{\sqrt{8}}, \frac{1}{\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{2}}, \frac{1}{\sqrt{8}}, \frac{1}{\sqrt{2}}, \frac{1}{2}, \frac{1}{\sqrt{2}}\right)$. The matrix T* has entries {0, ±1} and
$T^* = P_4.\ A_{12}.\ A_{11}.\ A_1$.

The digital hardware is realized using Xilinx ise and FPGA. The hardware is obtained by RTL schematic. This structure has 14 adder circuits and no shift operation. The Null multiplicative method is achieved.

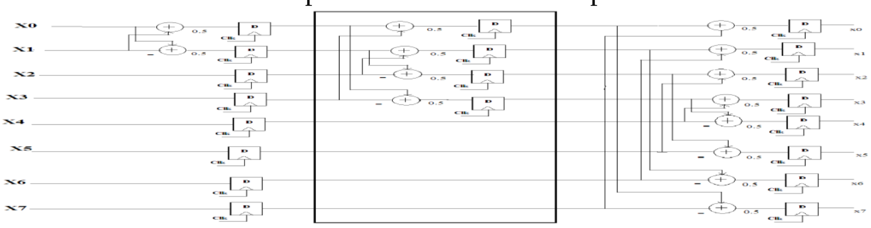

Figure.3. Multiplier-less circuit employing 14 adders

3. RESULTS AND DISCUSSION OF PROPOSED SYSTEM USING MODELSIM

Simulation In Modelsim: The Image in hexadecimal format (as numbers) is given as input in the coding. The obtained result is the binary output of the image after compression. Various simulations of the existing techniques are discussed below.

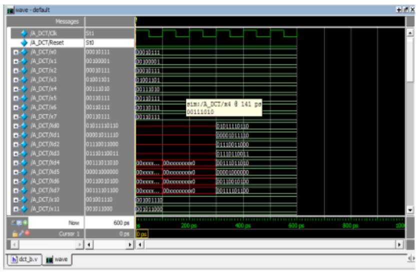

Figure.4.BAS 2008 simulation output

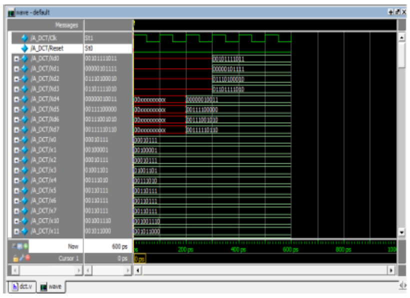

Figure.5.BAS 2011 output

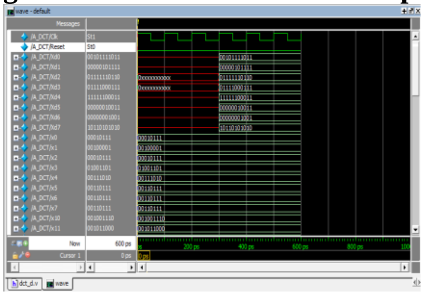

Figure.6.CB 2011 approximate DCT output

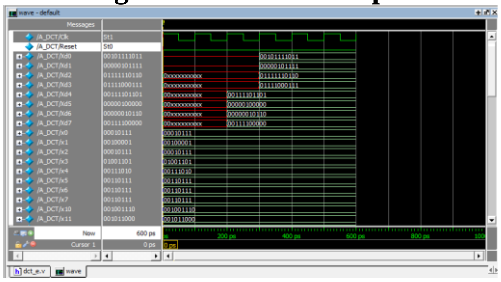

Figure.7.Modified CB 2011 approximate DCT output

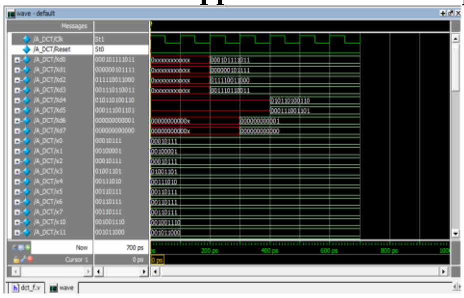

Figure.8. Approximate DCT output

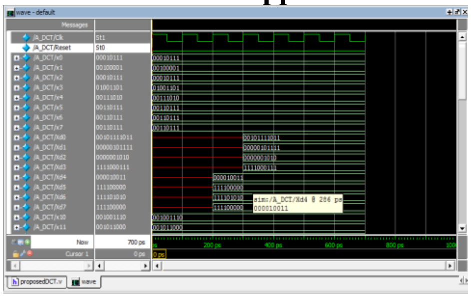

Figure.9. Proposed DCT output

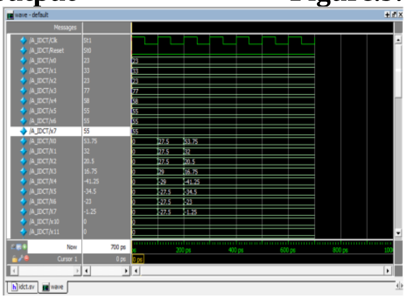

Figure.10.Inverse DCT output of proposed design

Performance In XILINX ISE: For comparative performance analysis, the proposed system is compared with the existing design. The following factors are analysed. The performance characteristics were analysed using Xilinx software. The device which was used to analyse the performance was xc6vsx475t-2ff1156. The results were also simulated using Modelsim6.3g. To analyse the performance of our device it was compared with four existing devices which were proposed earlier. From the below table, the numbers of IOB's used were reduced and also the clock delays of the signals were reduced.

Table.1.Result analysis of existing designs with the proposed work

Design name	No of Flip flops	No of Lut's	No of IOB'S	Clock delay
Bas approximate dct-2008	180	152	170	3.260NS
Bas approximate dct-2011	180	159	165	3.110NS
Cb approximate dct-2011	154	131	154	1.514NS
Modfied cb approximate dct-2011	164	130	159	2.001NS
Approximate dct-2012	96	103	164	2.203NS
Multiplierless circuit	182	120	144	1.414NS

Table.2.Power Rating

Design name	Power
Bas approximate dct-2008	0.113W
Multliplierless circuit	0.083W

We are further working on the process of increasing the number of bits i.e. using 16X16 bits. A hardware implementation of the above proposed method is in progress.

4. CONCLUSION

The multiplier less circuits employing 14 add operations and the other existing designs are extensively studied. The hardware structure implementing 14 adder circuits with null multiplicative complexity is advantageous over the other designs because of the area efficiency, less delay, and low power consumption. The study can be extended based on other transformation techniques, parameters involved for its performance analysis under noisy environments.

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