ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

Robot Fault Diagnosis Using a Novel High Speed Double-Tail Comparator

D. Sivasamy[1*], M. Dev Anand[2], V. Krishnama Naidu[3]
[1]ECE, Jawaharlal Nehru Technological University, Hyderabad - 85, Andhra Pradesh, India
[2]Department of Mechanical Engineering, Noorul Islam University, Kanyakumari District, India
[3]ECE, GRIET, Hyderabad, Andhra Pradesh, India
***Corresponding author: E-Mail: sivasamy.d@gmail.com**

ABSTRACT

A new fully double-tail comparator using regeneration with small power consumption and high speed is proposed. The aimed analysis suits is based on placing two cross coupled control junction transistor along the input face of the double-tail comparator. This cross connected control transistors tones up the positive feedback which cuts down the delay time. Increasing the switching speed of the transistor is added to reduce the power dissipation. Circuit model has been designed in classic 0.18µm CMOS technology. As a result, circuit shows up to 40% low power intake and vice versa reduced fault rate.

KEY WORDS: Fault, Nano Robot Comparator, Cross Couple Transistors, regeneration, Switching Transistor, CMOS Technology.

1. INTRODUCTION

Comparator is the most widely utilized component part in many practical application like analog-to-digital converters, Phase Locked Loops (PLLs) and sensor amplifier. A comparator is same as that like of an active amplifier in which they have two inputs (inverting and non-inverting) and an output. The role of a CMOS comparator is to compare an input signal with a source signal which produces a binary signal output like encoder. Comparator uses back to back hybrid matched inverters to convert the voltage into computer output in a short time period of time. It is more ambitious to plan a high speed comparator with a little supply voltage.

The functioning of the comparator plays a crucial role in realization of high desegregation, low power, low price and good invention. Kickoff cancelation method adopted by Yong-Bin Kim reduces the offset electric potential by using a computer controlled standardization technique. Raja (2012) suggested electron sharing circuit topology in which the repeated change of memory element comparator works at high speed and low power. Heung Jun (2004) looked into dynamic comparator by contributing two electronic converters within the input and output stage, in which regenerative latch strength is bettered. Shinkel (2007) declared oneself an efficient comparator, which uses back to back latch stage to induce positive feedback. These circuits are used in SRAM, sensor amplifier.

The left section of the article is prepared as follows. Section II supplies the procedure of the formal double-tail comparator and section III provides the functioning of the suggested double-tail Comparator. Computer simulated prototype results are showed in section IV and conclusion is drawn in section V.

1.1. Regenerative Comparator: A formal double-tail is shown in Figure 1. The primary reward of double-tail comparator is that they can control in lower supply voltage and has less piling. This double tail comparator has two tails Mtail1 and Mtail2 for quicker procedure and lower offset. The functioning of the double-tail comparator is. During readjust phase charging of transistors (M3-M4) takes place. Both the chase transistors are in off state. When clock =0, both the transistors MR1 and MR2 starts to discharge. During the regeneration phase both the chase transistors are in on state. When clock = VDD, firing of voltage takes place according to the IMtail1 and input voltages given at the transistors M1 and M2. Cross couple transistor supply a protection to input and output, this reduces the kickback noise.

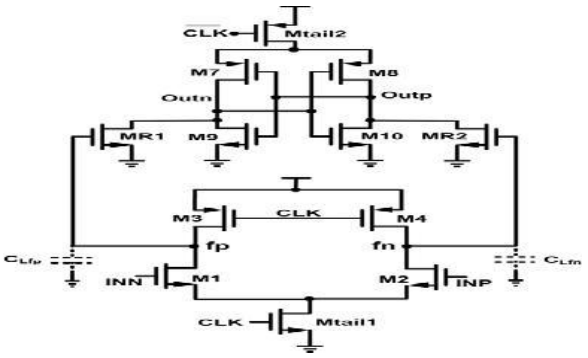

Fig.1.Conventional Double-Tail Comparator

The time lag of this double-tail comparator is due to the two principal parts .one is on account of the load capacitance and early because of the latch re-formation clock. The crucial portion to be noted is that, during the reset phase charging of nodes from zero to VDD lets in the power consumption. Also the efficient trans- conductance of the latch is not bettered.

1.2. Effective Double - Tail Comparator: Fig. 2 demonstrate the formal diagram of the proposed double-tail comparator. The designed Double-tail comparator shows a improve carrying into action which are applied in low voltage actions. The basic idea of this double-tail comparator is to speed up the latch positive feedback. Thus to speed up the latch regeneration we contribute two cross coupled controlled transistors (Mc1 and Mc2) on the input side of the comparator.

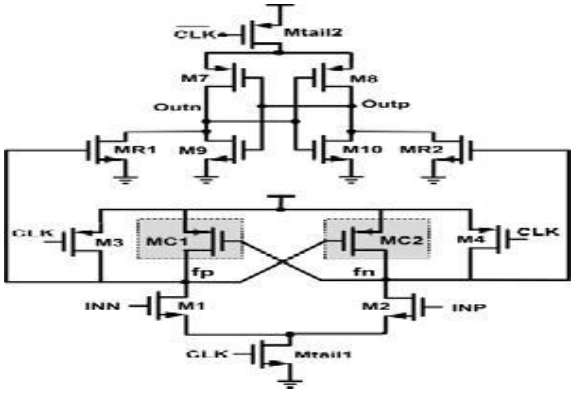

Fig.2.Effective Double-Tail Comparator

The activity of the proposed double-tail comparator is as complies. During reset level, both the tail transistors are in off state. When clock = 0, control transistors Mc1 and Mc2 are shifted off. Transistors MR1 and MR2 resets the output to the zero. During the regeneration phase (Clock=VDD) both the transistors M3 and M4 are turned off. Granting to the input voltages the node fn and fp starts to discharge. If input INP is heavier than INN, then fn cuts down faster than fp, this creates the control transistors Mc1 to turn on, extracts fp backs to the VDD. This makes the fnto discharge totally while other control transistors Mc2 stays in off state. The activity is vice versa when INN is greater than INP. Contempt of this good idea, the crucial component to be noted is that when one of the control transistors is in on state, this leads to flow of current from VDD to ground resulting in static power consumption. To prevent this static power consumption two NMOS transistors are contributed below the input stages (MSW1 and MSW2). The final structure of the double-tail comparator is indicated in Fig. 3.

During the reset phase, pre-charging goes on from the node to VDD in which both the switching Junction transistor is closed. During conclusion establishing phase one of the nodes is discharge allowing to the input voltage and to control transistors discover the node which successively speeds up the discharge rate. Hence, shifting transistor closes the early side of the node and grants the complete firing without any static power consumption. Thus switching transistors and control transistors competes the latch procedure.

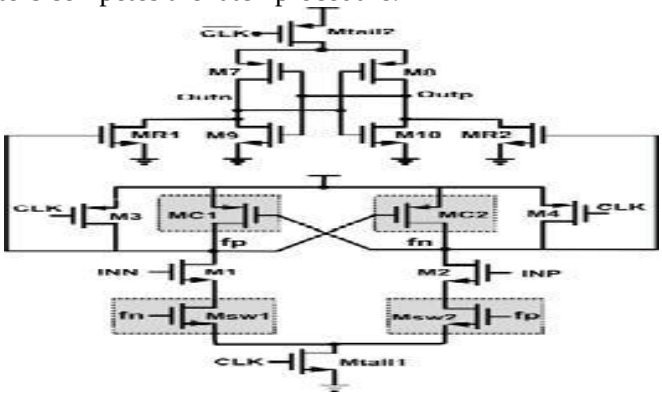

Fig.3.Final Structure of Double-Tail Comparator

2. SIMULATION RESULTS

The powerful double-tail comparator was planned and simulated in Tanner EDA tool using classic 0.18µm CMOS Technology We have consider each transistor as nano motors of the robot, delays all are error in the systems.

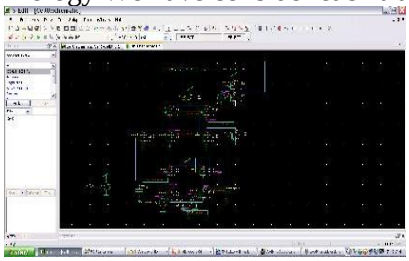

Fig.4.Conventional Represent of Double-Tail Comparator

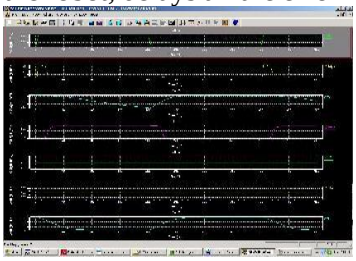

Fig.5.Output Wave Shape of Double-Tail Comparator

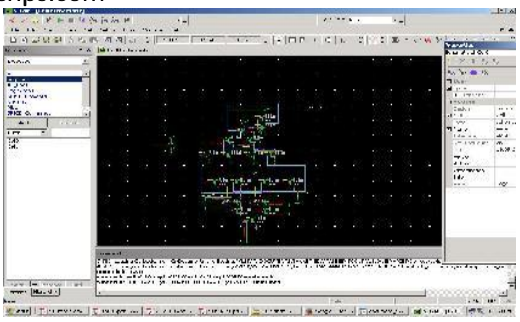

Fig.6.Schematic Layout of Aimed Double-Tail Comparator

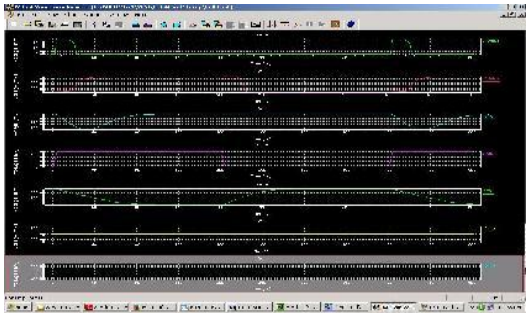

Fig.7.Output Waveform of Proposed Double- Tail Comparator

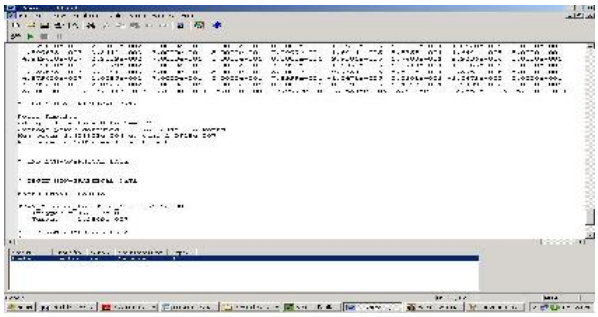

Fig.8.Error and Power Measurement of Conventional Double- Tail Comparator

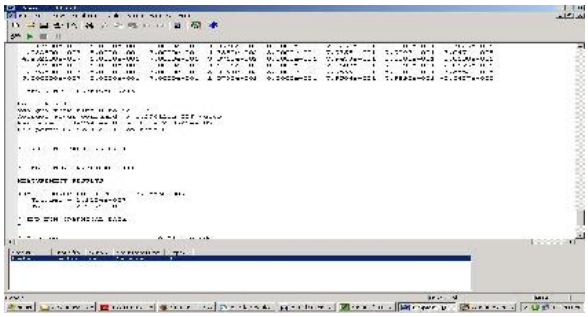

Fig.9.Error and Power Measurement of Proposed Double-Tail Comparator

Fig. 8 depicts the Error measurement of double- tail comparator and also the total power consumption of the circuit. Fig. 9 proves the Error and power measurement of the proposed efficient double-tail comparator. The comparison investigation is shown in the Table 1.

Table.1.Comparison error

Comparator Structure	Conventional Double-Tail Comparator	Aimed Double-Tail Comparator
Technology CMOS	180nm	180nm
Supply Voltage	0.8v	0.8v
Power Consumption	14µW	12µW
Error Measurement	7.6ns	7.4ns

3. CONCLUSION

A novel effective double-tail comparator with less power consumption and little Error was planned for the better performance of the comparator. The total evaluated Error of the proposed double-tail comparator comes out to be 7.4ns which is less than the previous double-tail comparator. Also, the power consumption of the proposed design is to be 12µW which is less than the previous double-tail comparator having a power consumption of 15µW. this will be applied in encoder part of the conventional robot.

REFERENCES

Heung Jun Jeon, Yong-Bin Kim, A Low-Offset High-Speed Double-Tail Dual-Rail Dynamic Latched Comparator, Proceedings of the 20th symposium on Great lakes symposium on VLSI, GLSVLSI '10, 2010, 45-48

Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman, Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18 µm CMOS Process, International Journal of Information and Electronics Engineering, 2 (6), 2012, 944 – 947

Shinkel D, Mensink E, Klumperink E, Van Tuijl E, and Nauta B, A Double-Tail Latch-Type Voltage Sense amplifier with 18ps Setup + Hold Time, in Proceedings IEEE Solid-State Circuits Conference, Digital Technology Papers, 2007, 314–315.