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Look Ahead Clock gating using an Auto gated Flip flop for Low Power Application

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ABSTRACT

We propose new technique for clock gating. Clock gating is helpful for reducing power consumed in digital system. There are three technique used (i) Synthesis Based method (ii) Data driver Method (iii) Auto gated flip flop (AGFF). The Auto gated Flip flop can be distributed in the clock distribution Network. Clock distribution use current other than voltage by giving global clock. With auto gated flip flop. It is used for power sowing. Clock gating can be tested in current mode pulsed flip flop with enable (CMPFFE) using 48nm CMOS technology. Look Ahead clock gating (LACG) computers the clock signal at one cycle ahead of time. Flip flop depends on the present cycle. This model can be characters by power saved in FF. This technique is based a data to clock togging. Majority of FF fall in positive Region Experimentation in industry- scale data display 22.5% reduction of clock power.

KEY WORDS: Look-Ahead Clock Gating (LACG), Auto-Gated FFs (AGFF), Current-Mode Pulsed Flip-Flop with Enable (CMPFFE).

1. INTRODUCTION

All portable Electronic devices require long battery life. Power consumption major problem in electronic products. Low power design is responsible to tolerate the power consumption clock signals are responsible for 30% to 60% of the total dynamic (switching) power consumption. There are many technique used to reduce dynamic power. Clock gating is one of the predominate techniques to reduce power. When a Logic unit is clocked its upcoming sequential elements receive the clock signal whether clock signal is needed or not. By means of clock gating Logic gates, Logic system architecture are employee at all stages we know above method is synthesis based.

Synthesis based clock gating is used in EDA tools. The abducing clock pulses can be measured by data to clock toggling Ratio. The clock enacting signals are derived by Logic synthesis. It is shown in data toggle in very Low rate compared to the gated clocks. The clock load consumes more power.

In order to address data driven clock gating the clock signal driving a FF is gated when there is No change in the clock cycle. The relation between data driver based and synthesis based clock gating method shown in Arithmetic circuits. The data driver gating is explained in Fig (1) disabled clock can be find in next cycle using a FF by the output with present input then the output will display in next cycle. The output of XOR gate are OR ed together for joint gating

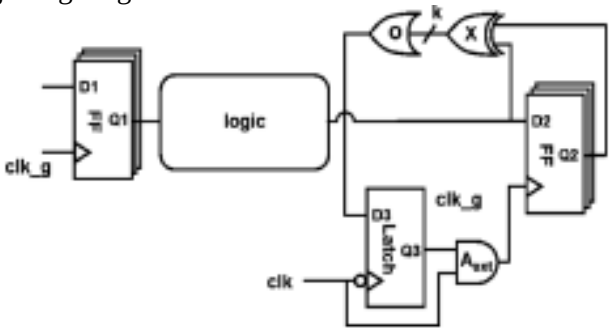

Fig.1. Circuit implementation of data – driven clock gating

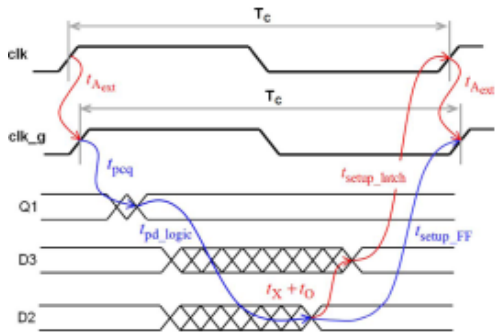

Fig.2. Sequencing of gating logic in data driven Clock gating

Data driven gating is suffered by short time- window. Clock gating is explained in Fig2. Design methodology is very difficult in data driven method. In order to maximize the power saving flip flop are grouped together. The main applications are unknown redundant clock pulses may increase in specific application. IP providers who are delivering RIT code need to broadcast the gating circuitry as per customer. It requires marinating different version of same IP.

In this paper we propose look Ahead clock Gating (LACG). It shows clock enabling signal at each flip flop depends on present cycle data same as data driven gating AGFF and data driven enable full clock signal. Data Driven requires optimization of FF. The simplified gating implementation is Auto gated Flip flop.

The Rest of the paper discussed about the optimization and implementation LACG section develops power saving models.

2. EXPERIMENTAL

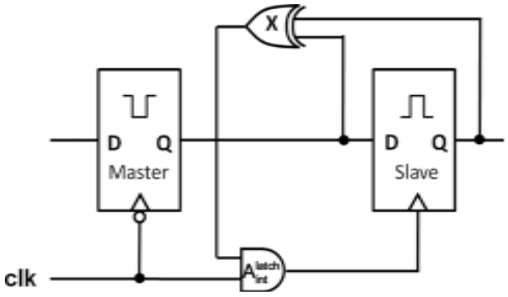

Fig.3. A gated Flip - Flop

Overview of Autogated Flip flop: The basic circuit diagram of Autogated flip flop is shown in Fig 3. The flip flop master latches are transparent in falling edge of the clock. The output must be stable. When master latch is opaque then EXOR gate indicate shows batch is change in state.

Power reduction was proposed for register based small circuits. The counters are the input for each Flip flop. There are two major draw backs is (i) show are gated but half of the clock load not gated. (ii) Timing constraints are imposed on those flip flop on critical path this avoids gating.

LACG uses AGFF for three goals. In order to stop the clock pulses in master Latch, making the clock pulse applicable for general design and avoiding timing constraints LACG is based on XOR output. The XOR output valid only during a narrow window [$-t_{setup}$, t_{ccq}] where t setup and t_{ccq} are FF's setup time. If t_{ccq} delay the XOR output and turns to zero XOR and OR gate are helpful in clock switching.

Fig4 represent how LACC operator assume FF^{11} as target and FF^{1} as source. The target depends on $K \geq 1$of source FF's.The source FFs can be found by a transversal of the Logic paths for D^{11}. It perform RTL or NOT-list description. Generate the enable signal obtained from t and its validity is t +1. The clock edge falling ad t +0.5 then D^{111} $(t+0.5) = \sum_{\times}(o^{11})x(t)$ since FF^{111} is opposite to clock. The signal Q^{111} is stable when the time period [t + 0.5, t +1]. By using FF for gating the consumption of power will be its own. In fig 4 identity that FF^{111} is clocked oppositely. Here internal XOR gate will be connected between D^{111} and $Q^{111.}$

LACG has a full clock cycle. In order to evaluate clock. For implementation require clock enabling signal. The timing diagram is explained below.

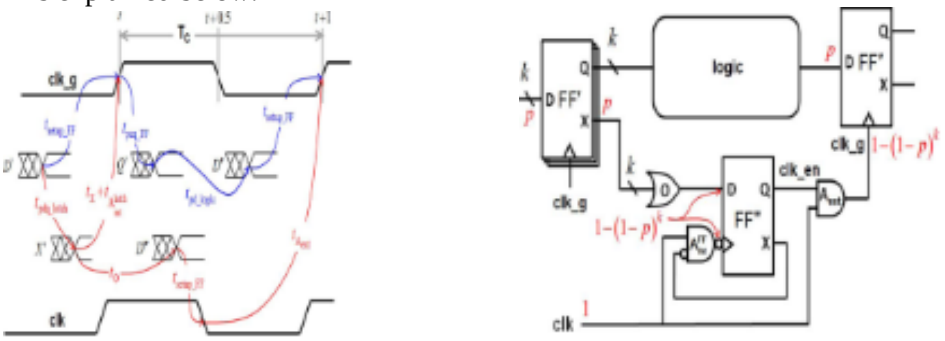

Fig.4. LACG of general logic

$$t_{pdq}\text{latch} + t_{Aint}^{Latch+tx} \leq t\ \text{setup}\ \ FF \quad \text{---------- 1}$$

Where t_{pdq}, $t_x$and t_A^{Latch} are output propagation delay, t_{setup} and FF is setup time.

$$t_0 + t_{\ setup}f_p + t_{pcq}\text{-ff} + t_{Aext} < T_c + t_x + t_{Aint}^{Latch} \quad \text{---------- 2}$$

There equation 2 is independent of timing circuit. The clock enabling signal is propagated from t setup – FF time window. As mentioned earlier $\sum x(D11)\times(t) = 0$ is sufficient clock D11 can be evaluated then D11 (t+1) = D11 (t). There will be a question have large. $Pr[(D^{11}(t+1)=D^{11}(t)\Lambda(\sum x(D^{11} \times(t)=1)]$

Thus LACG is power savor analyzed by worst-case toggling independence model from the theoretical approval power saving is analyzed.

Methodology of power saving: Current mode signaling scheme perform current to voltage and obtain voltage mode clock signal current mode is integrated with if that directly consume CM signal in order to reduce power consumption. The clock gating can be implemented into the current model signaling shown in the Fig 6.

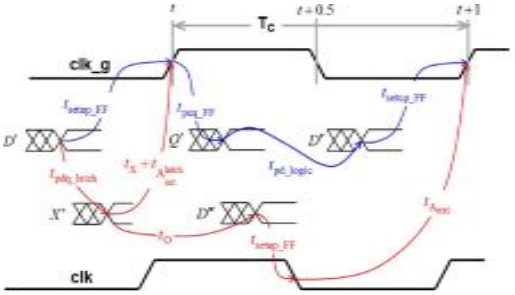

Fig.5. Previous CM schemes used an expensive transmpedance amp Rx which could in significant skew due to Vcm Shift if applied to CDNs

Current mode pulsed flip flop with Enable is the advance technology in current mode CMPFFE perform well other than CM signaling. CMPFEF similar to CM signal but here uses action low enable (EN) and If uses current – comparator. CC is a static storage call. A small signal analysis is expressed in CMPFFE.

$$Zin = \frac{1}{gm1+gm2} \quad ---3$$

In CMPFFE the transfer provides a push – pull current LACG is implemented in between CMPFFE. The transmitter receives voltage and clock signal can be controlled by clock gating. Then the current will distributed equally to all CMPFFE mode. In Fig 7 transmitter circuit uses NAND – NOR design.

Fig-7 The proposed CM Tx and CDN converts an VM input signal to a push – pull current with minimal interconnects voltage swing and distributes current equally to the CMPFFEs and (b) simulation waveforms confirm a VM input is converted to a constant CDN voltage and a represent push-pul current at each CMPFTE.

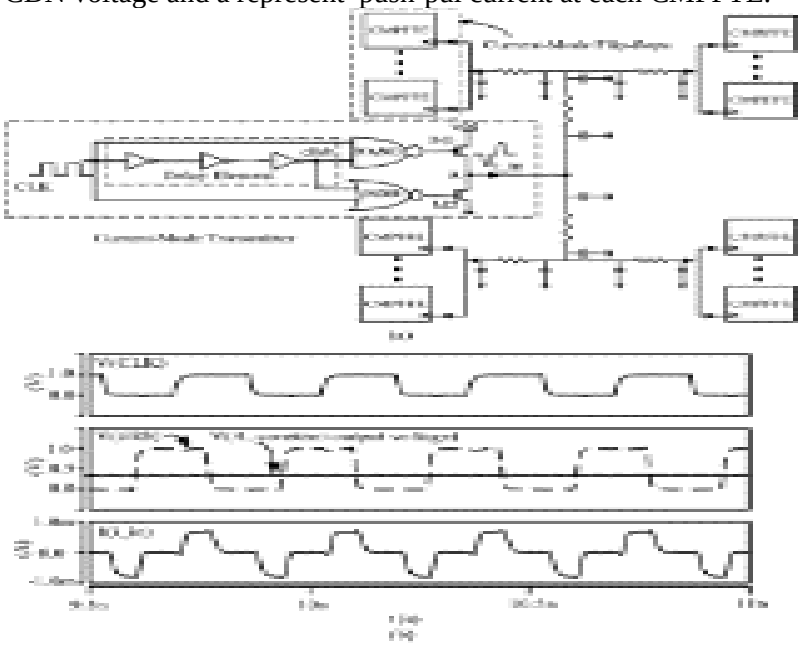

Fig.6. Timing sequence of LACG clock gating

Here PMOS change from the supply then the NMOS will be in off state. Simultaneously NOR gate willies the negative clock then NMOS will sink with current. While the M1 is off the PMOS get charged. Then Non- over login signal from the NAND – NOR will remove any short circuit current from transistor.

When the FF are toggled then

$$Pr[\sum_{xCD11} x(t) = 0] = (1\text{-}P)^k \quad \text{---------- 4}$$

The Actual power obtained from the following Analysis

$$Pr\ [\sum_{xCD11} x(1) = 1 \Lambda x11(6+1) = 0]$$

$$= [1-(1-p)^k](1-p) \quad \text{---------- 5}$$

In order to consulate LACG consider toggling as shown in the fig 4 the target of the FF will be

$$\{2(1-p)^k - [1-(1-p)^k]\} \frac{Cff + CLK}{3} - Pcx$$

$$= [3(1-p)^{k-1}] \frac{Cff + CLK}{3} - Pcx \quad \text{---------- 6}$$

Summing up all the above component the following result will be obtained.

$$[1-(1-p)^k]\ cff + C_{Aint} + C_{Aint} + [1=(1-p)^k + Kp] \quad \text{---------- 7}$$

from 6 and 7 rearrangement gives

$$C^{Save}_{dyn} = (1-p)^k (cff + clk + cff + co) - p(cx + kco) - \frac{Cff + CLK}{3} + C_{A\,int} + cff + Co] \text{ ---------- } 8$$

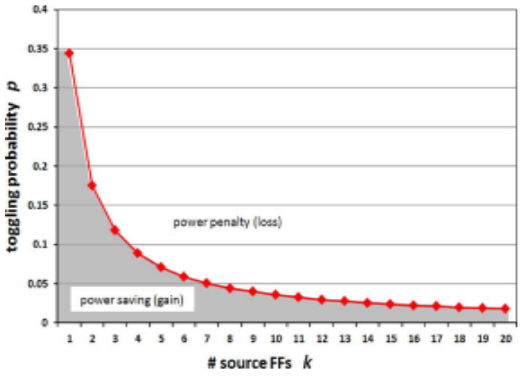

Fig.7. Power saving breakeven curve

Table.1. Typical capacitance in 20 Nm process Technology values in 10^{-15} f

C_{ff}	C_{CLK}	C_{ff}+ CL_K	C_Y	C_o	C_{Aint}
25-7	31.5	35-9	2.9	3.1	1.7

Experiments for minimizing logic gates: From the equation 8 C^{Save} are decreasing with the increase of P and K substitute C^{save} = 0 in eqn 8 dependency between P and q from the fig (7) and from the table (1) we take 20 nm process technology library. When the (k,p) points fall in the curved LACG will. Lose power the capacitance measured in 10^{-5}.

To develop logic sharing model to minimize the gating cost. OR logic increase the amount of redundant clock pulses. Since the clock is driven by Automating. The efficiency of the OR logic depends on best case and worst case. In CMPFFE input transition is 50% and output transition is 50%. The CMPFFE have lower clock – Q delay. The Monto carcoa simulation of clk – Q delay of Autogated clock gating is shown in fig 9.

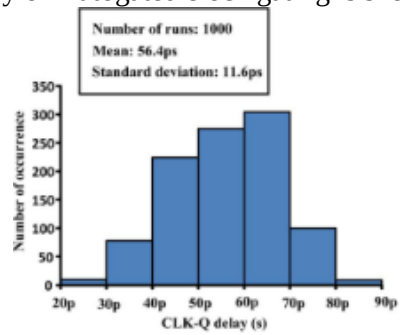

Fig.8. CLK-Q delay(s) vs Number of occurance

The flip flop power will not represent the overall power consumption of current mode. Power saving can be shown in CMPFFE when total power despite the additional static power.

The maximum cost perfect matching (MCPM) algorithm used to satisfy wcc (i) = 0 then the gating logic of ffi and ffj are not merged. A heuristic solution was proposed by LACG successfully.

3. RESULTS

Experimentation Result: The LACG is implemental with CMPFFE and power can be saved there are control blocks. With register file dynamic power is 80% and static power is 20%. The gating technology represented in Fig 4 is verified by EDA tool and original circuit was introduced. Clock gating technology employed by the design there LACG is a gate-level gating technology. Then power can be reduce power saving is explained in following graph fig 10.

In fig 10 clock c_{dyn} is 4770 of which 1060 pf has been reduced by LACG total dynamic power reduction is 22% power saving is achieved only by LACG. The dynamic powers depend on logic and static power independent of switching activity. The static power is 21% of total power taking all factors into account 22% of clock c_{dyn} reductions was translated into 12.5% reduction of total power.

CONCLUSION

Look ahead clock gating explained is very helpful for reducing. Clock switching power. Clock signal avoids timing constraints from existing clock gating technology closed model of the power saving technique by Auto gated Flip flop is implemented in gating logic. The gating logic will optimize the FF for joint gating. While in this paper

discussed power can be saved when global clock is given into the logic gates costuming of ff by group and yield high power saving this matter left for further research.

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