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An Enhanced Technique for Leakage Reduction in 8:1 Domino Multiplexer

S. Lakshmi Narayanan*, R. Jaya Nandhini, Dr. ReebaKorah
Department of ECE, Anna University, Chennai,Tamil Nadu, India.
***Corresponding Author: E.Mail:narayananrevs@gmail.com**

ABSTRACT

In conventional years, the dynamic power dissipation is dominant in CMOS technology. As the technology trims down to sub nanometer technology, the static power dissipation becomes dominant. Domino logic circuits with wide fan-in have many applications in digital signal processors, microprocessors and dynamic memory. Even though there are many applications, the static power dissipation becomes a consequential problem. To overcome this problem, a new domino 8:1 multiplexer with leakage reduction has been proposed which results in 74.03% and 73.9% diminution of subthreshold leakage in standby mode when compared with Footless standard domino multiplexer and Footed standard domino multiplexer and these are designed and simulated using tanner EDA tool under 250 nm technology.

Keywords: dynamic power dissipation, static power dissipation, suthres hold leakage, CMOS.

INTRODUCTION

CMOS logic design has been mainly classified into Static logic and Dynamic logic. In static logic, the outputs are generated in response to the output and it can preserve its output as long as there is power supply. In dynamic logic, the outputs rely on the charge temporarily stored in the parasitic capacitance. The dynamic logic needs less area when compared with the static complementary logic. Because the static complementary logic needs 2N number of transistors and the dynamic logic needs N+2 number of transistors for N input logic. But it leads to cascading problem and charge sharing problem stated in. To minimize this problem, domino logic is improved. An inverter is present to overcome the cascading problem and it also has a keeper transistor to latch the output to high level. It has two phases. They are pre charge and evaluation phase. During precharge phase, the clock becomes low and the domino node is pre charged to v_{dd} which results in low output. During evaluation phase, the clock becomes high and the output depends on the NMOS logic block. Eventhough the domino logic requires less area, it leads to dynamic and static power dissipation.

The static power dissipation is mainly due to the subthreshold leakage because of sub nanometer technology. Then the leakage can be reduced by many techniques. One effective technique is Power Switching. During the sleep mode, it shuts down the two sleep transistors. So there will be no path from vdd to ground which reduces the subthreshold leakage. Another technique is Reverse Body Biasing is explained in. By Reverse body biasing the substrate, the threshold voltage can be increased which reduces the leakage.

LITERATURE REVIEW:

8:1 Model of Multiplexer of Standard Domino Structure: The standard domino 8:1 multiplexer with footer transistor is shown in the Fig.1. It consists of two phases. They are precharge phase and evaluation phase.

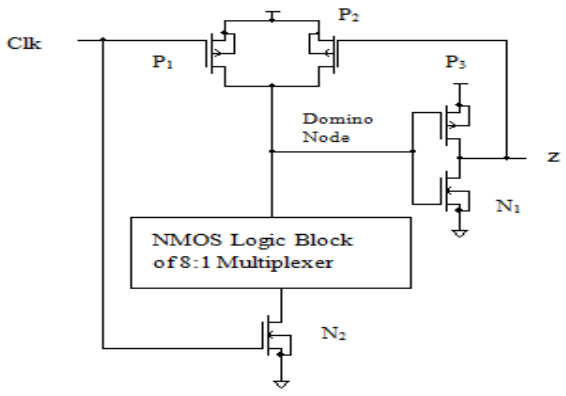

Fig.1. 8:1 Multiplexer of Standard Domino with Footer Transistor

During precharge phase, the clock is low and the transistors P_1 and N_2 are switched ON and OFF respectively. As a result the domino node is precharged to vdd and the output node Z is low. In evaluation phase, the clk is high and the transistors P_1 and N_2 are switched OFF and ON respectively. At the beginning of evaluation phase, the transistor P_2 is switched ON because of the feedback of precharge phase output and this leads to contention i.e. the transistor P_2 is trying to charge the domino node but at the same time the NMOS logic block is trying to discharge the node which leads to delay.

8:1 Multiplexer of Standard Domino without Footer Transistor: The standard domino 8:1 multiplexer without footer transistor is shown in the Fig.2. It comprises of two phases which are precharge phase and evaluation phase.

During precharge phase, the clk is low and the transistor P_1 is switched ON. As a result the domino node is precharged to vdd and the output node Z is low. During evaluation phase, the clk becomes high and the transistors P_1 is turned OFF. At the starting of evaluation phase, the transistor P_2 is turned ON because the precharge phase value 0 is given as feedback to the transistor P_2 and this leads to contention i.e. the NMOS logic block is trying to discharge the node but the transistor P_2 is trying to charge the domino node simultaneously that is the drawback which increases the delay time but the required number of transistors is less than the 8:1 Mux of Standard Domino with Footer Transistor.

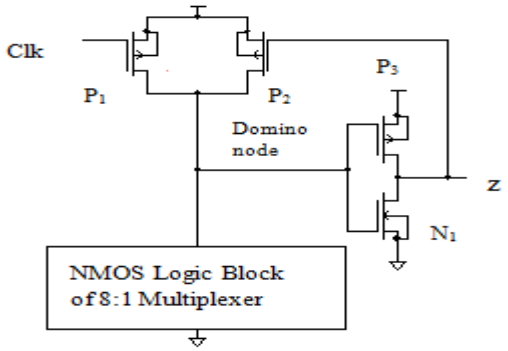

Fig.2. 8:1 Multiplexer of Standard Domino without Footer Transistor

PROPOSED WORK

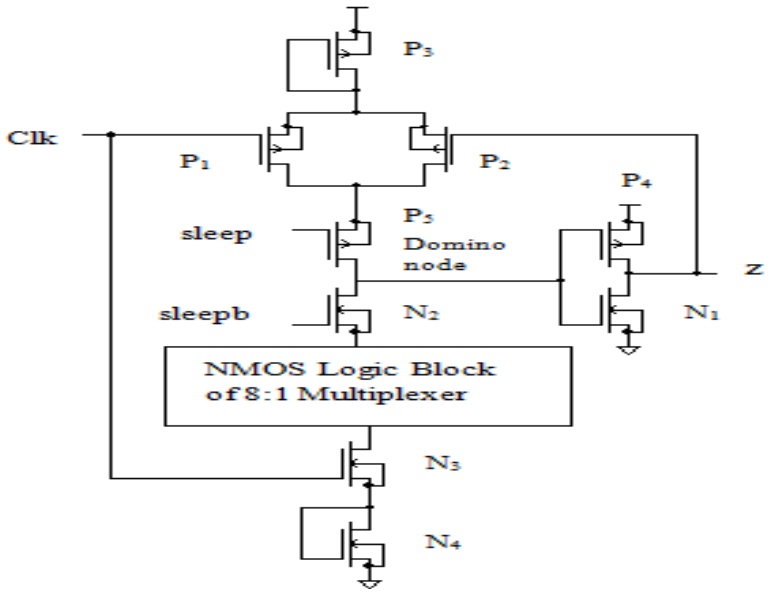

Fig.3. 8:1 Domino Multiplexer with Leakage Reduction

A new technique for leakage reduction in 8:1 Domino Multiplexer is shown in the Fig.3. It has two modes. They are active mode and standby mode. During active mode, the sleep is low and sleepb is high and the transistors P_5 and N_2 are in ON condition. During precharge phase, the clk becomes low and the transistor P_1 gets switched ON and N_3 gets

turned OFF. As a result, the domino node is precharged to vdd and the output node Z is low. During evaluation phase, the clk becomes high and the output Z depends on the NMOS logic block. During standby mode, the sleep is high and sleepb is low and the transistors P_5 and N_2 are in OFF condition. Because of this, the stacking effect is created and it provides resistance between the power supply and ground which reduces the subthreshold leakage and the diode connected transistors are also used to reduce the leakage in sleep mode.

RESULTS AND CONCLUSION

Results: The proposed system is designed and simulated using tanner EDA tool under 250nm technology which is shown in the Fig.4 and Fig.5.

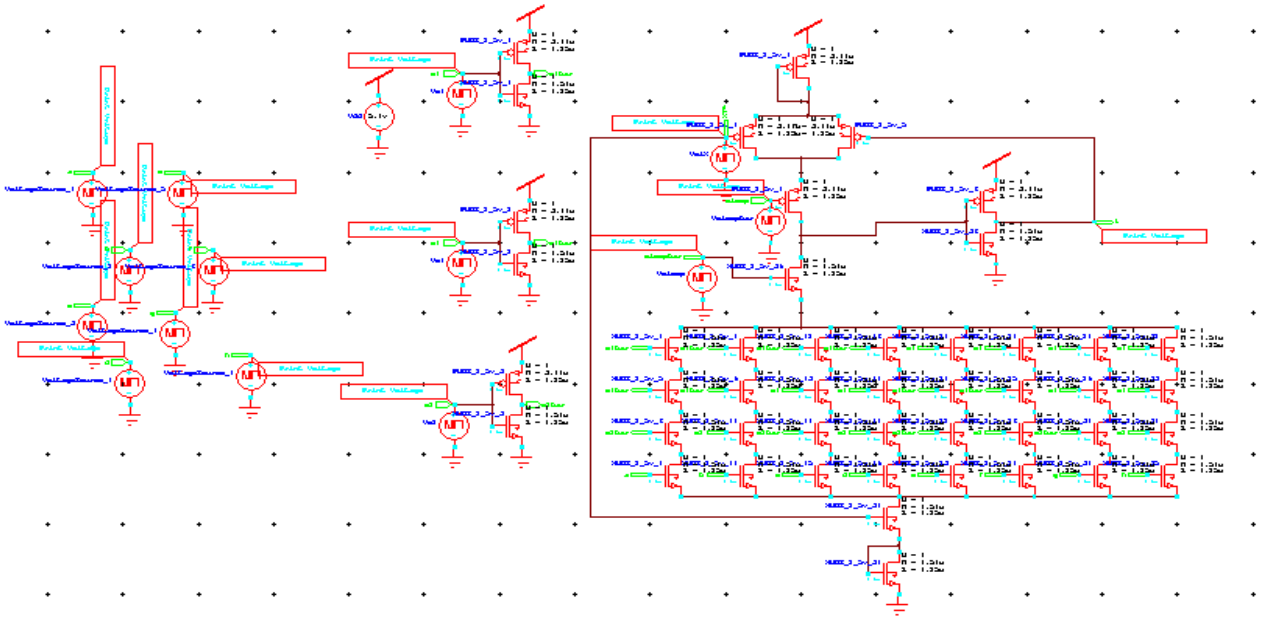

Fig.4. Schematic of proposed System

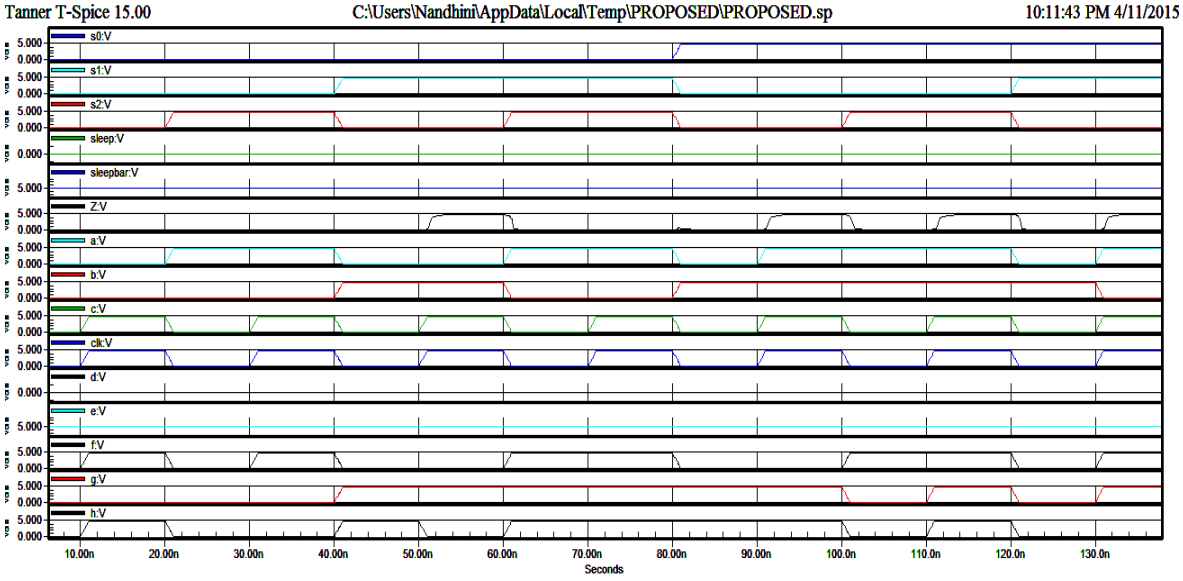

Fig.5. Simulation Result of Proposed System

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The table 1 and 2 infers that the power consumption of proposed system is more in active mode and less in standby mode which is shown in the Fig.6 and Fig.7. Then the subthreshold leakage is more in active mode but very much less in standby mode which is shown in the Fig.8 and Fig.9. But the drawback is that the proposed system leads to minimum delay which is shown in the table 3 and Fig.10.

Table.1.Comparison table of power consumption in active mode and standby mode

S.No.	Various Domino Logics	Power Consumption in Active Mode	Power Consumption in Standby Mode
1.	Standard Domino 8:1 Mux with Footer Transistor	4.80e-4 W	1.401e-2 W
2.	Standard Domino 8:1 Mux without Footer Transistor	1.299e-3 W	1.412e-2 W
3.	Proposed System	7.33e-4 W	1.153e-2 W

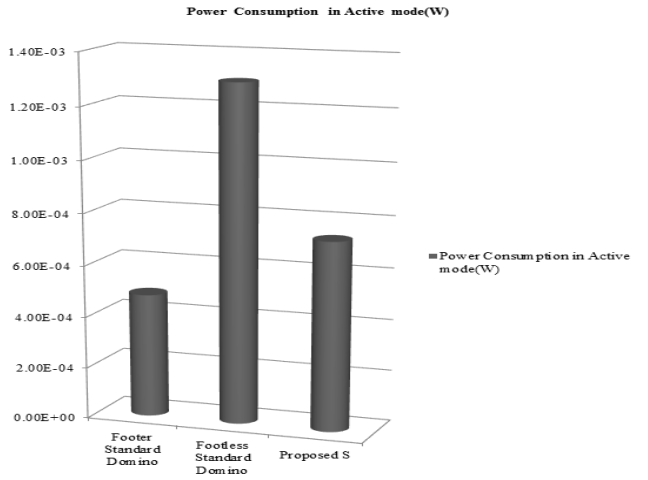

Fig.6. Comparison Graph of Power Consumption in Active mode

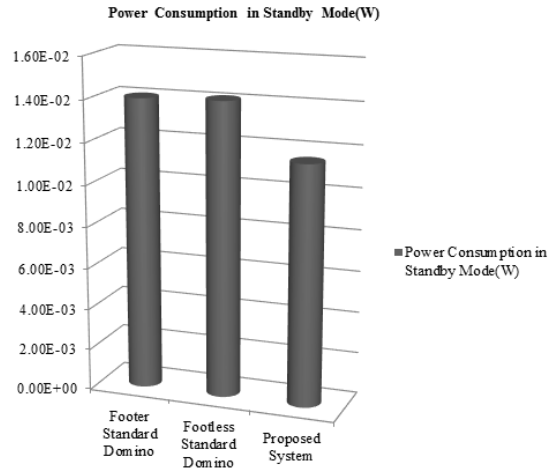

Fig.7.Comparison Graph of Power Consumption in Standby mode

Table.2.Comparison table of subthreshold leakage in active and standby mode

S.No.	Various Domino Logics	Subthreshold Leakage in Active Mode (pA)	Subthreshold Leakage in Standby Mode (pA)
1.	Standard Domino 8:1 Mux with Footer Transistor	103.5	28.88
2.	Standard Domino 8:1 Mux without Footer Transistor	134.5	28.75
3.	Proposed System	443.6	7.5

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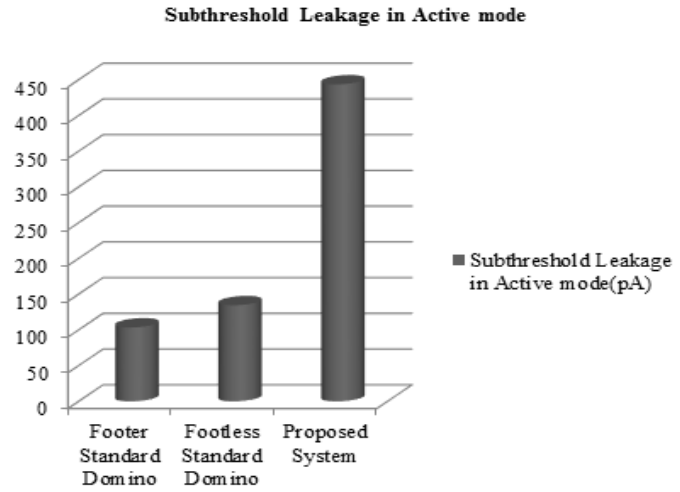

Fig.8.Comparison Graph of Subthreshold Leakage in Active mode

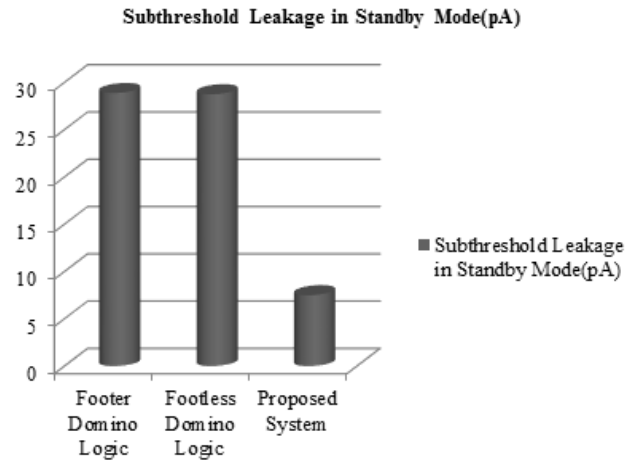

Fig.9.Comparison Graph of Subthreshold Leakage in Standby mode

Table.3.Comparison table for delay time in active mode

S.No.	Various Domino Logics	Delay time in Active Mode (ns)
1.	Standard Domino 8:1 Mux with Footer Transistor	30.23
2.	Standard Domino 8:1 Mux without Footer Transistor	30.32
3.	Proposed System	30.67

Figure.10.Comparison Graph of Delaytime for Various Domino Logics

CONCLUSION

Wide fan-in domino multiplexer is used in home stereo applications, microprocessors and digital signal processing. But it has both static power dissipation as well as dynamic power dissipation. In conventional years, the dynamic power dissipation is dominant but nowadays the static leakage becomes dominant because of the subnanometer

regime. With this purpose a new 8:1 domino multiplexer has been proposed to reduce the subthreshold leakage in standby mode.

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