Journal of Chemical and Pharmaceutical Sciences ISSN: 0974-2115

An efficacious technique to reduce leakage current in 9T SRAM Cell

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ABSTRACT

As per growing technology, the rise of Static power consumption due to frequent scaling of technology leads to increase in Sub-threshold leakage current, largely with lower threshold voltage for achieving higher efficiency. Though, the leakage current becomes the main contributors for larger power dissipation of circuits in memories. From the various sources of leakage currents, the major leakage power occurs only due to the subthreshold leakage current flowing through the circuit during standby mode. Low power applications, minimizing the leakage current in memories is critical. In this paper, a new leakage reduction technique is proposed for achieving low leakage reduction in Standby mode. It is deprived of being penalized in power and delay performance. It shows that proposed 9T SRAM cell reduces leakage current by a substantial amount related to conventional 9T SRAM and existing method. Simulation is performed in 45 nm technology in Tanner EDA tool.

Keywords: SRAM cell, Static power, Leakage power, Sub threshold leakage, semiconductor memories, Threshold Voltage.

INTRODUCTION

SRAM (Static Random Access memory) is one of the read or write memory circuits that allows the alteration of data bits which are stored in memory cells. One of the main features of SRAM is its high speed and hence it is used as main memory in supercomputers or cache memory in mainframe computers. SRAMs contribute to major power dissipation. Latches are used for storage of data in SRAM. Shortage of leak again SRAM will prevents faster advancements in the performance of the computer. SRAM cell is made of two inverters cross coupled each other that acts like a latch. They are used to store each bit of information and also no need to refresh the circuit. The SRAM has more reliability and resource of power. It is commonly applied to computer microprocessors that the chips are performing various calculations and processing is explained. They are immensely developed thus results in increasing density also the temperature gets affected and so low power memory upsurges. For the advancement of SRAM cell providing better stability, hence it is essential to deal with low leakage power savings. In an SRAM cell, leakage current is flowing from bitlines and bit cell.

Previous work:

Conventional 9T SRAM: It shows the structure of 9T SRAM cell where the standard 6T bit cell is designed along with additional three transistors were engaged in nine transistor 9T SRAM cell. It consists of two sub circuits with top and bottom located. The above four transistors with inverters circuit part is basically a 6T SRAM cell. The word line signal controls the bit line transistors. The values of data stores in the top part of the SRAM memory circuit. While the bottom part of a circuit is formed of both bit line as well as read signal transistor. Normally there are two operations performed here. For both operations, the bit lines are set to required values and the transistor N2 is connected to the read signal RBL. Access transistor operation is entirely depends on the values stored in their nodes.

Forced Stack: A technique for reducing leakage power is the forced stack approach. Here the existing transistors are divided into two halved transistors, so that there is an emergence of stack effect that leads to leakage reduction. There will be a small amount of leakage takes place due to two off devices than one device in off condition. When more than one transistor in the stack is turned off, that is known as "Stacking effect". By setting the input as '0', both the transistors are getting turned off, thenthe intermediate node voltage is generated due to the small amount of drain current flowing into the circuit. But, this voltage is larger than the Vg due to theex is tence internal resistance at the transistor N3. Thus leakage has been reduced by stack effect [6].When two or more transistors are turned off together, reverse bias current is induced between them and it results in the reduction of sub-threshold current. While retaining the state, there will be huge leakage power gets saved. As the transistors are separated delay overhead occurs.

Journal of Chemical and Pharmaceutical Sciences ISSN: 0974-2115

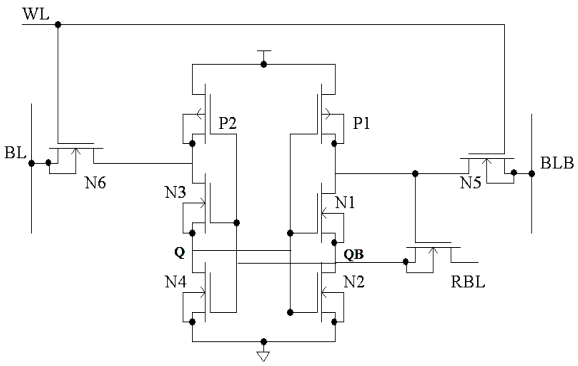

Fig.1.Conventional 9T SRAM

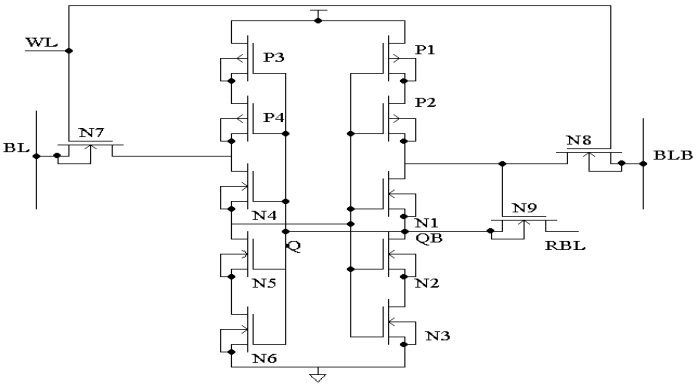

Fig.2.Forced Transistor Stacking

PROPOSED WORK

In this proposed technique, there are two processes takes place. One is biasing the source and the other one is providing bias to the wordlines. This technique is most appropriate for reducing leakage in standby mode. Here's a pull down transistor N8 is connected to the gate terminal of the bitline transistor N5 which is connected to the word line is presented in. In active mode by locating the wordline high, will increase the gate voltage. While in standby mode, the wordline must be kept low which makes the transistor M7 in off condition. Once the wordline gets is not selected, a voltage is applied to the bitlines which may block the leakage current flowing through the region. There will be an appearance of body effect and thus causes the threshold voltage to be higher and the sub threshold leakage has been reduced drastically. Also the stability will be preserved while reducing the leakage. Thus, by applying the technique wordline and bitline will cause the leakage to be reduced considerably.

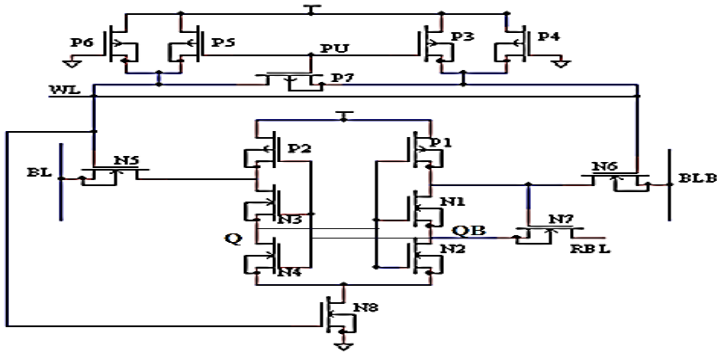

Fig.3.Proposed Technique design

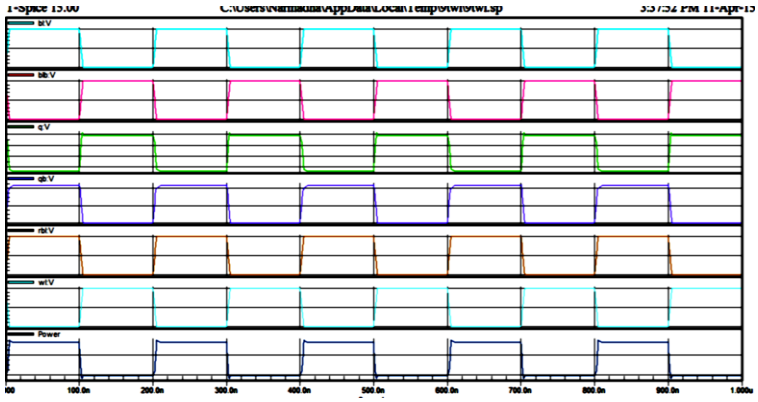

Fig.4.Output of Proposed Technique

Journal of Chemical and Pharmaceutical Sciences ISSN: 0974-2115

Table.1.Illuminates power consumed and delay in active mode and leakage in idle mode

Techniques	Active Mode		Standby Mode
	Power (In Watts)	Delay (In ns)	Sub-threshold Leakage Current (In Amps)
Conventional 9T SRAM	2.29E-005	95.20	310.6mA
Forced Stack	2.46E-008	104.98	151.1 µA
Proposed Technique	9.45E-005	102.9	21.27µA

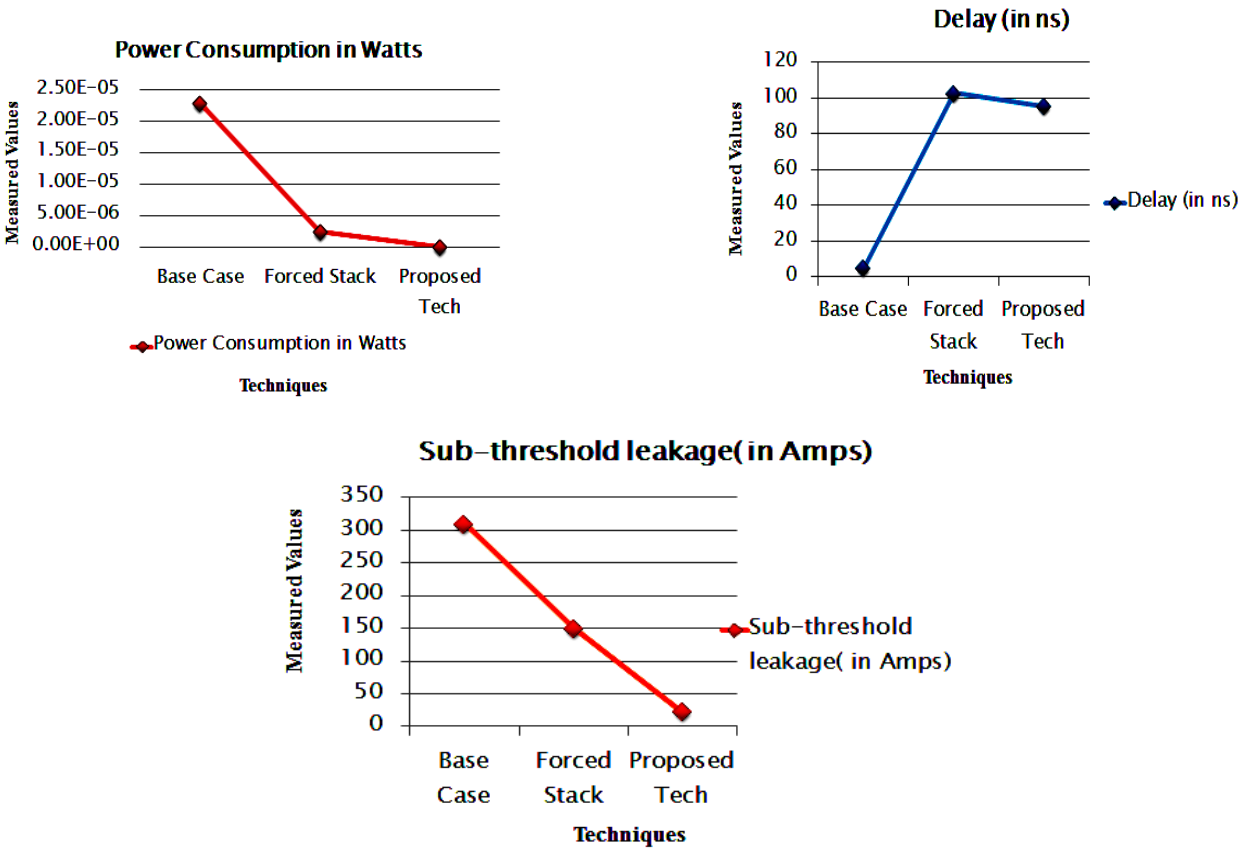

Fig.5.Illuminates the amount of power consumed, delay and Sub-threshold leakage existing technique at the 45nm technology in active and standby modes

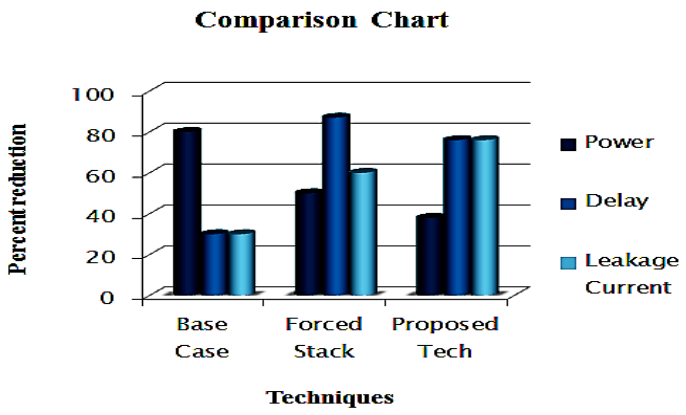

Fig.6.Illuminates the comparison chart of power, delay and Sub threshold leakage in active and standby modes

Journal of Chemical and Pharmaceutical Sciences ISSN: 0974-2115

CONCLUSION

In Scaled nanometer technology, the sub-threshold leakage current is a foremost challenge. In this paper, the Conventional 9T SRAM cell is designed and simulated using Tanner at 45 nm Technology for low leakage. It demonstrates that the leakage current has been reduced drastically in comparison to the Conventional 9T SRAM cell and existing Forced stack approach with minimal delay and power trade off. Therefore, if the wordline and bitline leakage has been reduced the overall cell leakage will be a significant amount of leakage reduction.

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