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# Implementation of Master Slave Flip-Flop and Latches in VLSI Circuits

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## ABSTRACT

In modern VLSI circuits power optimization is censoriously more consequential for low power applications such as clock gating, internal memory partitioning. While designing latches and flip-flops in modern VLSI circuits, optimization of the power is interpretative because large amount of power is consumed when the input transition do change the state. This paper reveals alternative of MS flip-flop with Hybrid Latch flip-flop, Semi-dynamic flip-flop, Sense Amplifier flip-flop to reduce the transistor size and to reduce power consumption of the flip-flops. The proposed Master Slave flip-flop is compared with some other flip-flop and characteristics for the different digital circuit is studied with various parameters such as transistor count, parasitic value and power dissipation. These parameters are simulated using Tanner EDA 250nm technology.

**Keywords:** Power optimization, Flip-flop and Latches.

## INTRODUCTION

Low power consumptionhas become eminently an important issue in modern VLSI circuits. Power Optimization refers to the problem of reducing power consumption in a digital circuit. Various techniques such as transistor and gate sizing, clocking, pass transistors are used to reduce the power, As technology develops the complexity of the system also increases, This gives rise to power consumption, which is a great issue faced by the world today. One of the causes for high power dissipation is rapid switching of internal signals. Various techniques are used to avoid rapid switching of internal signals. Power consumption of latches and flip flops is one of the provocations to consume power. Several researches have worked on low power flip-flop design, but they are mostly concentrated on one or few types of flip-flop and latches. Flip-flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Basic elements used for storing information are flip-flops and latches. In latches outputs are repeatedly affected by their input as long as the enable signal is not asserted. Flip-flops change their outputs only when the rising and falling edges of the enable signal. Normally controlling clock signal is the enable signal. Several techniques to reduce the dynamic power have been developed of which clock gating is predominant. It is foremost to save power in these latches and flip-flops without compromising the state integrity or performance. This paper presents an approach to minimize the power consumption in flip-flop and latches. Analysis is done on several existing designs and the modifications are done on the proposed design by clubbing various latches and flip-flop with modified P-flip-flop. Normally a P type flip-flop selectively functions in D-type flip-flop mode or latch mode depending on its clock signal input. The proposed design is explained along with working, its advantages, and application and so on. The results are simulated and concluded along with the future scope.

## EXISTING DESIGNS

**HLFF (Hybrid Latch Flip-Flop):** HLFF is one of the supersonic flip-flop structures. This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This sharp pulse is generated at the positive edge of the clock using clock and delayed version of clock. It includes a negative pulse generation unit, a latch flip-flop, a buffer unit, a sample unit and a hold time. It is resilient to clock signal slopes, but it does have appositive hold time.

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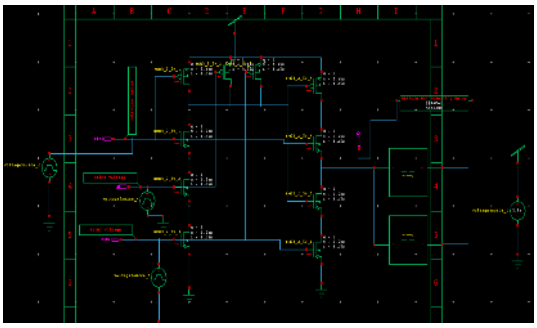

**Figure.1.NOT gate using CMOS for HLFF**

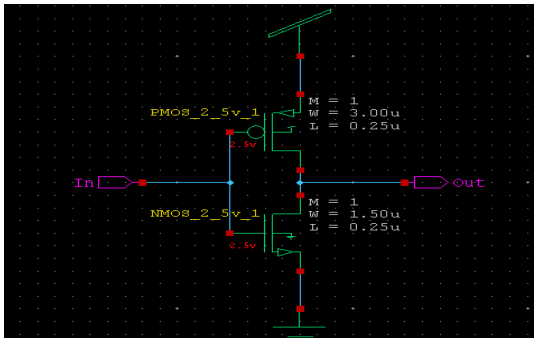


**Figure.2. Schematic Circuit of HLFF**

It is difficult for a Keeper circuit to perform well over a range of different operations of supply voltage levels because keeper strength should be comparatively weak for low supply voltages and stronger for higher operating voltages. So a strong keeper is craved for higher supply levels to obtain good noise, robustness. This is very suitable for high performance system. Fewer transistors are employed in the HLFF, which gives rise to low power consumption. It exhibits better soft_clock edge properties. In this circuit two clock signals and one D are used as input signals. Output Q will be obtained before the keeper circuit. Clock bar signal is the inverted form of the original clock signal; here three inverters are used to provide the complement of the clock signal. When the clock signal is high then the output will follows the input, here the sharp pulses are obtained.The propagation time of three inverters defines the transparency window. The glitch is produced in the transparency window at the first stage. It can be easily noticed that it is formed by three inputs CMOS NAND gate which has the functionality for wanted glitch generation. Second stage of the circuit captures the generated glitch. If the glitch has not appeared the output is brought to zero. In this circuit unnecessary internal transitions appeared as a consequence which elevates the total power consumption of the flip-flop. To avoid these disadvantages this flip-flop is combined with modified P flip-flop, then the results are obtained at the proposed design section.

**SDFF (Semidynamic Flip-Flop):** Semi dynamic is an hybrid flip-flop with rapid structures having large clock load and large effective pre-charge capacitance.SDFF consumes a slightly high power due to large effective precharge. Eventhough it needs high power,this is well suited for high performance design. This circuit is designed of a dynamic front end and a static back end. NAND gate is a logical gate which provides an output that falls only if all the inputs are true. Complement to that of NAND gate is AND gate. A LOW output results only if the both inputs to the gate are HIGH;A HIGH output results only if both the input to the gate are LOW. This flip-flop samples input D and produces complement output. Q bar is the logic complement of D. On the falling edge of the clock the flip-flop enters the pre-charge phase, the node near the keeper circuit pre-charge high, cutting on node Q from the input stage.

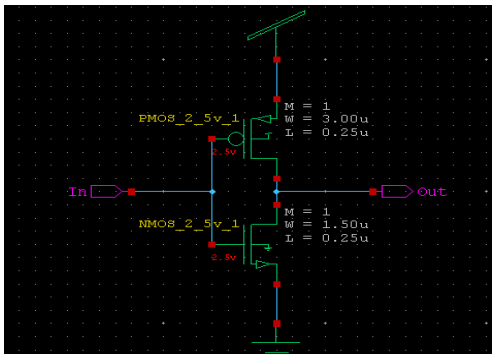


**Figure.3. NOT gate using CMOS**

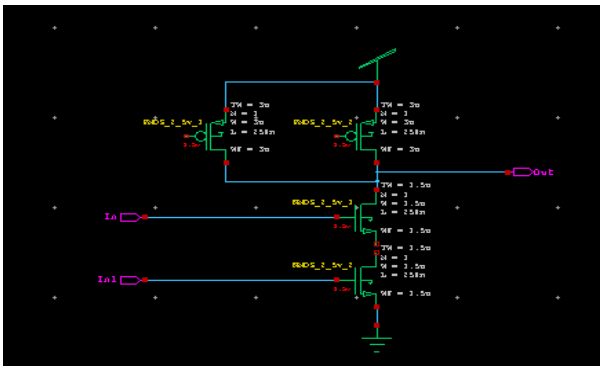


**Figure.4.NAND gate using CMOS**

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The inverter present near the output act as a static latch and it holds the previous logic level of Q and Qbar. Since the second clock signal is also low during pre-charge, the output of the NAND gate remains high and the holding the transistor N1 ON. The evaluation phase begins with the rising edge of the clock. If the input D is low the node nearer the keeper circuit remain high, it is held by inverter latch. Node Q would either remain low or will be discharged through transistors N4 and N5, driving Qbar high. Three gate delays after clock raises, output of NAND gate will be low, turning transistor N1 off. This shut-off operation will prevent a subsequent low to high transition of D from the discharging node. This feature provides the flip-flop its edge triggered nature.

**SAFF (Sense Amplifier Flip-Flop):** Recent modifications of semi dynamic flip-flop exhibits very small delay,calculated as a sum of setup time and clock to output delay in high speed data path applications. This SAFF have differential outputs,and single or differential inputs can be used accordingly.

This flip-flop present a small clock load,since only three transistors are connected to the clock signal. Initial design includes sense amplifier in the first and the NAND based cross coupled SR latch in the second stage. This improves the output stage to reduce the overall delay.The sense amplifier stage is precharged during the interval when the clock signal given as the input is low. The high state of S bar and R bar keeps transistor N5 and N6 ON,charghing their sources upto Vdd-Vtn because there is no path to ground due to the off state of the clocked transistor.Since either N1 or N2 transistor is ON,the common mode of N2 and N6 is also precharged to Vdd-Vtn.Therefore prior to the leading clock edge,all the capacitance in the differential tree are recharged. Rising edge of the clock generates falling transistion on only one of sense amplifier outputs Sbar or Rbar. This negative pulse is being captured by the SR latch and held until the end of the cycle.

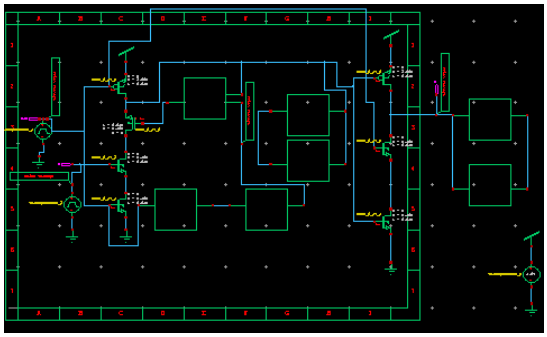

**Figure.5.Schematic circuit of semi dynamic flip-flop**

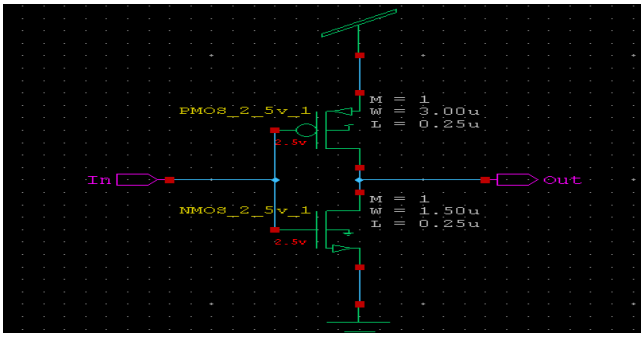


**Figure.6.NOT gate using CMOS**

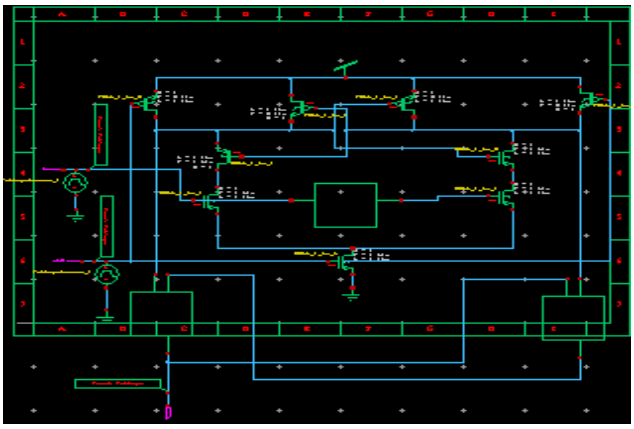

**Figure.7.Schematic circuit of sense amplifier flip-flop**

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**PROPOSED DESIGN**

P-HLFF:P-HL flip-flop is an alternative of Master slave flip flop, it is used in high speed applications. At the rising edges of the clock both the transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter. The switching power at node Z can be reduced due to diminished voltage sink. In this design, Modified P flip-flop is clubbed with the HLFF and the output results are taken for the analysis Jayagowri (2011). Here the output of the modified flip-flop is taken as the input of the HLFF. When the clock value is HIGH, then the output follows the output. Two inverters are connected back to back, it acts as a buffer for the circuit. The node which is situated behind the buffer circuit driven the output Q. HLFF samples the data on one edge of the clock and eliminates thee delay of the data flow.Thus the delay is rectified in the circuit, it enhances the performance ofthe clubbed circuit. HLFF operation is similar to that of the latch because it delivers the soft clock edge. P-HLFF is designed by clubbing modified pulse and hybrid latch flip-flop.This results in better performance and high power consumption.

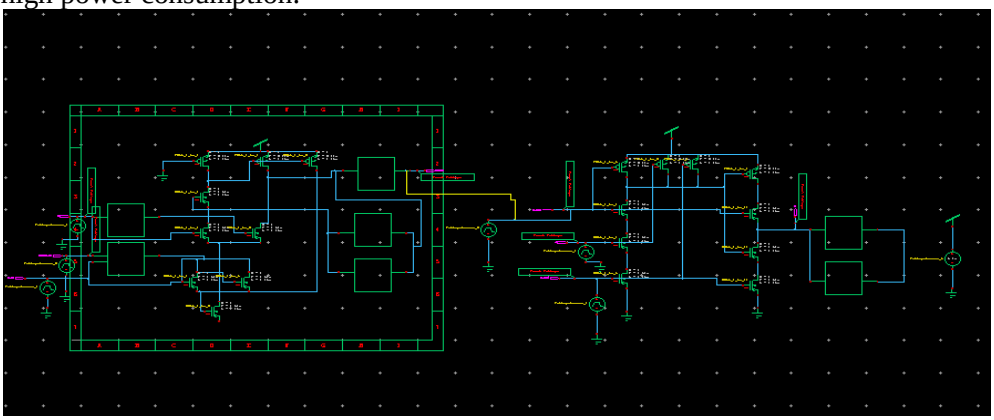

**Figure.8.Schematic circuit of P-HLFF**

P-SDFF:

P-SAFF:P-SAFF is modeled by clubbing Modified P flip-flop with SAFF. SAFF has low power consumption as well as less delay. Even though it having less delay and low power consumption, the output of this flip-flop is sometimes in floating state To avoid this clubbing is done with the Modified P flip-flop. Thus it improves the performance of the circuit and reduces the delay as well as power consumption. The simulation results are observed and mentioned below.

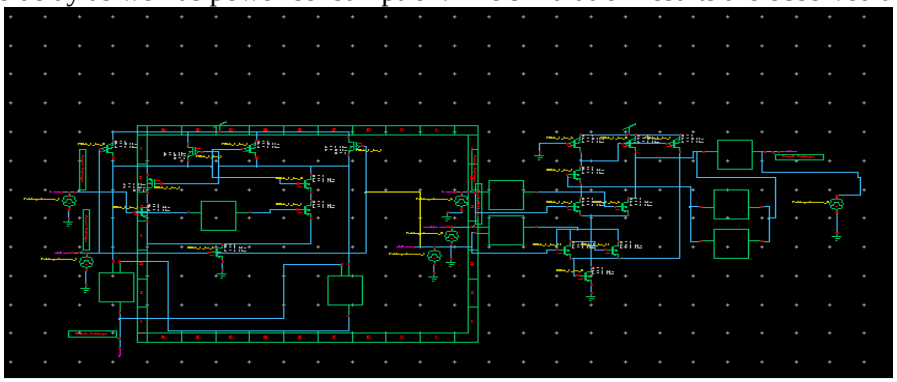

**Figure.9.Schematic of P-SAFF**

**RESULTS & DISCUSSION**

The various types of flip-flops were obtained from TANNER EDA in 250nm technology at room temperature. The supply voltage Vdd is 5v. Simulation result for the various designs is shown below. The power consumption is very high in above proposed Flip-flops. In the existing method number of transistors used is more than proposed design so the power consumption and delay gets increases. Normally power consumption is directly proportional to the number of transistors used. Lesser the number of transistors, power consumption is reduced. P-HLFF, P-SDFF, P-SAFF designs are used to reduce this power consumption. For the HLFF, number of transistors used in 17 and power

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consumption in 55mW. In the proposed P-HLFF, number of transistor used is reduced to 8 so the power consumption also reduced to13 mW. In the similar manner power consumption in P-SAFF is 16mW and P-SDFF is 15mw.

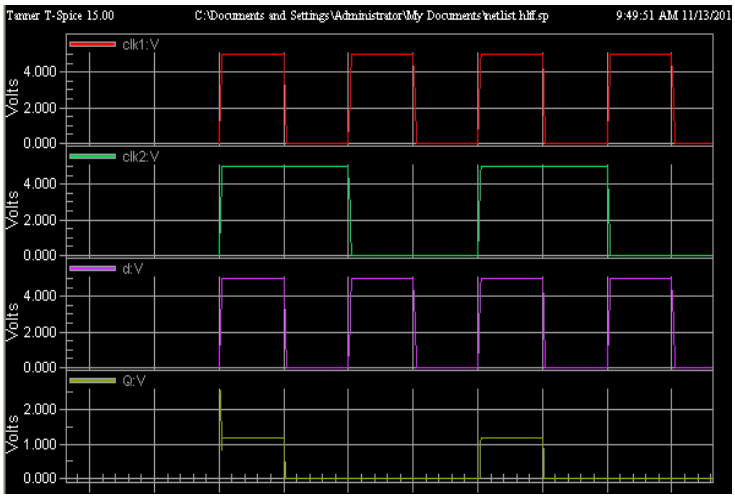


**Figure.10.Simulation result of HLFF**

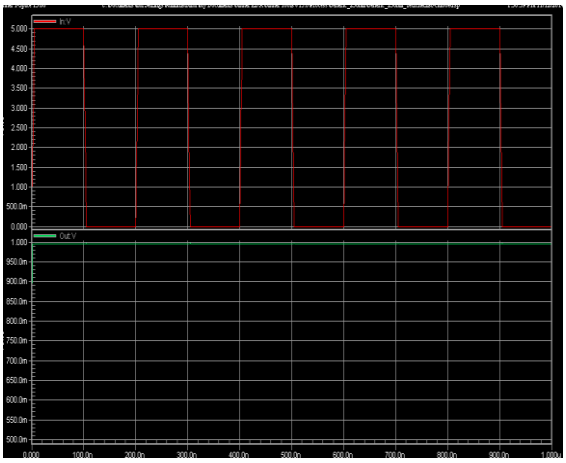

**Figure.11.Simulation result of P-HLFF**

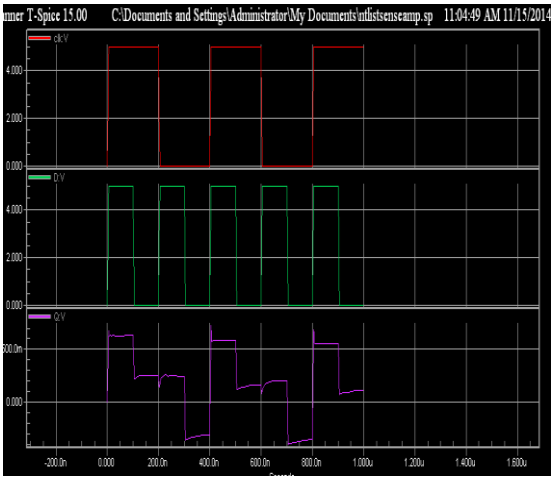


**Figure.12.simulation result of SDFF**

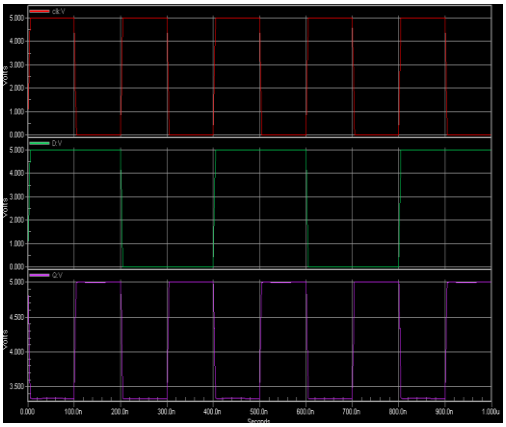

**Figure.13.Simulation result of SAFF**

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The various types of flip-flops were obtained from TANNER EDA in 250nm technology at room temperature. The supply voltage Vdd is 5v. Simulation result for the various designs is shown below. The power consumption is very high in above proposed Flip-flops. In the existing method number of transistors used is more than proposed design so the power consumption and delay gets increases. Normally power consumption is directly proportional to the number of transistors used. Lesser the number of transistors, power consumption is reduced. P-HLFF, P-SDFF,P-SAFF designs are used to reduce this power consumption. For the HLFF, number of transistors used is 17 andfor SDFF and SAFF the number of transistors used are 21 and 16 respectively. But for our proposed method the number transistors used are very much reduced. Transistor used for P-HLFF, P-SDFF, P-SAFF are 8, 5 and 7 respectively.

**Table.1 Performance of proposed system**

| Flip-Flop | HLFF | SDFF | SAFF | P-HLFF | P-SDFF | P-SAFF |
|---|---|---|---|---|---|---|
| **Power consumption(mW)** | 55 | 30 | 25 | 13 | 16 | 15 |
| **No-of-transistors** | 17 | 21 | 16 | 8 | 5 | 7 |
| **Delay(ps)** | 28 | 32 | 38 | 11 | 6 | 9 |

From this tabulation the power consumption is less in P-HLFF. Number of transistors are reduced in P-SDFF. Delay is reduced in P-SDFF, Comparing all these types P-SAFF have better performance than other flip-flop.

## CONCLUSION

In this paper, the various flip-flops design like,P-HLFF, P-SDFF, P-SAFF are discussed. These were been also designed in Tanner EDA tool and those result waveforms also discussed. The comparison table is also added to verify the designed methods. With these all the result the proposed flip-flops performed better than all other designs. Thus the power consumption of the proposed design is lowest because of shortest discharging path. By modifying the design, the power consumption can be lowered to the minimum level.

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